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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,929	10/05/2001	Jun Koyama	740756-2368	3139

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EXAMINER	
NELSON, ALECIA DIANE	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/970,929	KOYAMA ET AL.	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,37-54,73-90 and 109-126* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,37-54,73-90 and 109-126* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. ***Claims 1-18, 37-54, 73-90, and 109-126*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichikawa et al. (U.S. Patent no. 6,559,821) in view of Marshall et al. (U.S. Patent No. 6,121,760).

With reference to **claims 1, 10, 37, 46, 73, 82, 109, and 118**, Ichikawa et al. teaches a display device comprising: a source signal line driver circuit (1, 2) and a gate line driver circuit (3); a pixel portion (Figure 1), each of the source signal line driving circuit, gate line driving circuit, and the pixel portion provided over a substrate (see

Figure12, column 15, line 34-36), a shift register (1, 2) included in the source signal line driving circuit and gate line driver; a level shifter (332) included in the source and gate line drivers for converting a voltage amplitude of input signals (see column 14, lines 20-26); and a current source (385) provided for the source and gate line driving circuits for supplying a current to the level shifter (see column 16, lines 58-61) With further reference to **claims 73, 82, 109, and 118**, Ichikawa et al. teaches the usage of a decoder (393) included in the source and gate line driving circuits for outputting pulses in accordance with input signals.(see column 17, lines 8-13).

While teaching the usage of a shift register in the source and gate driving circuits, there fails to specific teaching of the shift register outputting pulses in accordance with clock signals, however this is conventional operation of a shift register and is well known by those skilled in the art. Further, Ichikawa et al. fails to teach that the current source supplies the current only when the shift register serially outputs the pulses or that the shift register (driving circuits) are comprised of a plurality of units..

Marshall et al. teaches a power regulator wherein a shift register, having a plurality of stages, or units (see column 2, lines 9-15), operates with respect to clock pulses from a clock signal in which the clock signals are generated in association with the power control pulses. That is upon initiation of the power regulator a fist clock signal is output to the shift register, the shift register output terminals are set to a first level and the shift register will output a signal on successive occurrences of the second clocking signal (see column 5, line 16-column 6, line 15).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the usage of the shift register with multiple stages wherein power is only provided when the shift register output pulses as taught by Marshall et al. in a device similar to that which is taught by Ichikawa et al. in order to thereby provide a display device in order to improve power regulation for reducing power consumption of the display.

With reference to **claims 2, 11, 28, 47, 74, 83, 110, and 119**, Ichikawa et al. teaches that the source and gate line driving circuits and the pixel portion are provided of a glass substrate (see column 15, lines 34-46).

With reference to **claims 3, 4, 12, 13, 39, 40, 48, 49, 75, 76, 84, 85, 111, 112, 120, and 121**, Ichikawa et al. teaches that the driving circuit is provided on the same substrate as the pixel portion (see Figure 12). While not specifically teaching that the driving circuits and the pixels circuits are disposed on different substrates, conventional display devices are well known to have this configuration.

With reference to **claims 5-9, 14-18, 41-45, 50-54, 77-81, 86-90, 113-117, and 122-126**, Ichikawa et al. teaches that the display device is a liquid crystal device (see column 6, lines 37-39), however fails to teach the types of devices that the display can be incorporated into. However, it is well known in the art for display device, preferably

LCD device to be incorporated into personal computers, portable information terminals, car audio sets, and digital cameras.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsueda teaches a display apparatus wherein the driving circuits are formed on the active matrix substrate or formed separated from each other, as well as a shift register outputting with respect to a clock signal.

Ishii et al. teaches a driving circuit of a display device wherein the shift register has a number of stages and outputs with respect to the clock signal. Wherein the pixel matrix and the driving circuitry is formed on one substrate.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (703) 306-0403. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
February 21, 2005

AMR A. AWAD
PRIMARY EXAMINER